

--Turning to Figure 2, one portion, section A, of the MCM module 10 depicted in

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Figure 1 is shown in greater detail. Specifically, Figure 2 presents an enlarged view of section A of the MCM module 10, and more specifically depicts the support base 12 having disposed thereon the decoupling capacitor 14 which is embedded within the interconnect layer 16. Figure 2 presents a cross-sectional view of this portion of the MCM device 10 which cross-sectional view illustrates that the MCM device 10 is a multilayer device. Figure 2 further shows that the decoupling capacitors 14 can be electrically coupled to the ground plane 29 and power plane 28 of the MCM module 10. In certain exemplary embodiments, the decoupling capacitor 14 may be connected in parallel with the power plane 28 and the ground plane 29. Figure 2 further depicts that the interconnect layer 16 can include a plurality of layers that can be organized into a pattern of circuit connections that can be employed for interconnecting the circuit devices 20 mounted to the surface 18 of the interconnect layer 16. Figure 2 further shows that the interconnect layer 16 can include power and ground connections, 31 and 33, that can provide power to the circuit devices 20 and which are decoupled by the decoupling capacitors 14.--

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Please replace the paragraph beginning at page 10, line 18, with the following rewritten paragraph:

--Figures 3A - 3B depict one particular embodiment of a decoupling capacitor 30

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that can be employed with the MCM 10 depicted in Figure 1. The depicted decoupling capacitor 30 is a component that is mounted to the support base 12 before the interconnect layer 16 is formed. The decoupling capacitor 30 can comprise a thin film MCM-D technology fabricated device, and in particular can be formed by multi-layer thin film processing with copper or aluminum metallization and SiO<sub>2</sub> dielectric material fabricated on a silicon based substrate. One such capacitor and techniques for forming such a capacitor is generally described in the above referenced U.S. Patent 5,134,539.--

Please replace the paragraph beginning at page 10, line 27, with the following rewritten paragraph:

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--Figure 3A provides an overhead view of the decoupling capacitor device 30 that is formed as a component level device and which is capable of decoupling a power plane and a ground plane for an MCM device. The decoupling capacitor 30 is a silicon base die decoupling capacitor with an embedded ground and power plane and a SiO<sub>2</sub> dielectric material disposed therebetween. The decoupling capacitor 30 can be sized and shaped for the application at hand, and the depicted decoupling capacitor 30 is not to be understood as an exhaustive representation of the structure of the decoupling capacitors suitable for use with the present invention. Moreover, other dielectric materials can be employed, and the type of dielectric will depend upon the application. It is understood however that the silicon material dielectric should provide good thermal expansion properties. As shown in Figure 3A the depicted decoupling capacitor 30 includes a first section 32 and a second section 34. Thus a given die can support more than one capacitor. The first section 32 of the depicted decoupling capacitor 30 comprises six individual capacitors each of which share a common ground plane. In this depicted embodiment, each of the six individual capacitors 36 are substantially the same size, thereby providing substantially the same capacitance. The second portion 34 of the depicted capacitor 30 comprises two capacitors 44 each of approximately the same size, and each larger than the individual capacitors 36 of the first portion 32. Accordingly, it will be understood that the individual capacitors 44 provide greater capacitance than the individual capacitors 36 of the first portion 32. The size and the shape of the capacitors can vary depending upon the application, and those of ordinary skill in the art will be able to select the proper capacitance for decoupling the circuit. Further, the distribution, arrangement of the capacitors can vary depending upon the application, and for example, separate capacitors, with separate ground planes can be employed for decoupling different circuit devices to for example allow separate decoupling of analog and digital circuit devices. These arrangements can vary depending upon the application.--

Please replace the paragraph beginning at page 11, line 24, with the following rewritten paragraph:

--For both capacitors 36 and 44, the top surface comprises a plurality of pads each of which can be employed for forming an electrical connection with the interconnect

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layer 16 that can be formed over these decoupling capacitors. Turning to Figure 3B a cross-sectional view is presented of these decoupling capacitors 36 and 44. Specifically, Figure 3B shows a silicon base 48 upon which a ground plane 50 is disposed. Above the ground plane is a power plane 52. Disposed between the power plane 52 and the ground plane 50 is a dielectric material which can be any suitable dielectric material such as SiO<sub>2</sub>, polyimide or any other suitable material. The ground planes 50 and power planes 52 can be formed of aluminum, copper, aluminum oxide or other conductive material. The power planes, ground planes and dielectric material can be stacked in layers to provide a selected capacitance appropriate for the application. As further shown by Figure 3B, gaps 54 can be disposed at locations within the power or ground planes that allow for separating the power and ground planes from each other thereby preventing a short circuit. The metal layers within the interconnect layer 16 can electrically couple to these pads, thereby connecting the circuit pattern to the power and ground planes at a location that is proximate to, or at, the location of the decoupling capacitors. This allows for minimizing the interconnect distance.--

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Please replace the paragraph beginning at page 13, line 28, with the following rewritten paragraph:

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--Figure 6 depicts that an interconnect layer 16 can be formed on top of the component layer. In one practice, an *in situ* process can be performed wherein a dielectric layer is directly deposited on the upper surface of the plurality of components, in this case the decoupling capacitors 14 and the resistive element 22. Further processing can include patterning and forming vias in the *in situ* formed dielectric layer. The vias can be disposed within this layer to expose at least some of the contact pads at the upper surface of the decoupling capacitors 14 and the resistive element 12. Such exposed contacts facilitate electrical connections to the connecting layers that can be later deposited. To this end, the forming of a metalization structure above the *in situ* processed dielectric can occur in a manner that allows metalization within the vias. Metal formed within the vias can create electrical connections to at least some of the contact pads exposed by the vias and carried on the surface of the components. For the interconnect layer 16 depicted in Figure 6, a plurality of layers have been deposited in

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sequence to form the circuit pattern. Accordingly, in subsequent steps further chip interconnect layers can be added by alternatively applying dielectric and metalization layers. Although photo patterning of the deposited dielectric layers provides one process for forming the interconnect layer 16, it will be understood by those of ordinary skill in the art that other techniques can be employed for depositing the interconnect layer and thereby forming the circuit pattern for the MCM device. Moreover, it will be understood by those with ordinary skill in the art that although the interconnect layer 16 depicted in Figure 6 is shown as having a plurality of metalized layers, that such a module can be formed with a single layer, or two layers, and that no specific number of layers is necessary for the practice of the invention. Additionally, it will be understood that in optional embodiments and practices, decoupling capacitors and other components, can be disposed between metallic layers, by placing these devices on the interconnect layer partially through the deposition process.--

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In the claims

Please amend claim 12 and add new claims 21-33 as follows:

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12. (Amended) A device for interconnecting a plurality of circuit devices, comprising:
- a support base having a first surface;
  - a decoupling capacitor mounted on said first surface; and
  - an interconnect layer having a pattern of circuit connections and being formed over said decoupling capacitor, whereby said decoupling capacitor is embedded within said interconnect layer,
- and whereby said pattern of circuit connections of said interconnect layer is coupled to said decoupling capacitor and a plurality of circuit devices mounted on a surface of said interconnect layer opposite said first surface of said support base.
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